


Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 01207P008C5	Application Number: Not yet assigned
	First Named Inventor: Peter M. Pani	10/811, 422
	Filing Date: Herewith	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
<i>MA</i>		4,020,469		Manning	4/26/77	
		4,661,901		Veneski	4/28/87	
		4,684,830		Tsui et al.	8/87	
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		4,870,302		Freeman	9/26/89	
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		5,256,918		Suzuki	10/93	
		5,260,610		Pedersen et al.	11/9/93	
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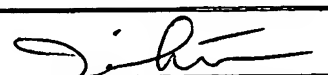
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		EP	0415542A1		Advanced Micro Devices, Inc.	3/6/91		
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		PCT	WO96/05964		Minnesota Mining and Manufacturing Co.	2/29/96		
		PCT	WO96/35261		BTR, Inc.	11/7/96		
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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
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UTA		Ping-Tsung Wang et al., "A High Performance FPGA with Hierarchical Interconnection Structure", Institute of Electrical and Electronic Engineers, pp. 239-242, May 30, 1994.	
UTA		Motorola Product Brief, "MPA10XX Field Programmable Gate Arrays", 4 pages total, September 27, 1993.	
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VTa		Sinan Kaptanoglu et al., "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages. <i>No date</i>	
VTa		Dave Bursky, "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy", Electronic Design, pp. 33-34, October 1, 1993.	
VTa		Dick L. Liu et al., "Design of Large Embedded CMOS PLA's for Built-In Self-Test", IEEE 1988, pp. 50-53.	
VTa		Xilinx, "The Programmable Gate Array Data Book", 1992.	
VTa		F. Zlotnick et al., "A High Performance Fine-Grained Approach to SRAM based FPGAs, Wescon '93 Record, pp. 321-326, September 28-30, 1993.	
VTa		Barry K. Britton et al., "Optimized Reconfigurable Cell Array Architecture for High Performance Field Programmable Gate Arrays", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.2.1-7.2.5.	

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